REMARKS

Claims 1-21 are pending. The Examiner's reconsideration of the objections and rejections in view of the amendments and remarks is respectfully requested.

The Examiner has objected to the drawings. The Examiner stated that the counters of claim 1 and the compiler of claim 12 must be shown or the feature(s) canceled from the claims(s).

Figure 3 has been amended to depict a first counter and a second counter as described at, for example, page 12, lines 6-7. No new matter is believed to have been entered.

Claim 12 has been amended to clarify the limitations therein. The word compiler has been canceled from the claim. The Examiner's reconsideration of the objection is respectfully requested.

The Examiner has objected to the Abstract and the Summary as possibly being inaccurate. The Abstract and Summary have been amended to clarify which instruction set is invoked by which branch instruction. The Examiner's reconsideration of the objection is respectfully requested.

The Examiner has objected to the specification as not describing the "unconditional switch branch instruction of the primary form". The Applicants respectfully disagree. For Example, at page 11, line 12, the specification states that "upon determining an unconditional switch branch instruction of the primary instruction form, the branch unit shifts the processor from the primary fetch/decode/issue mechanism 322-324 to the alternate mechanism for the alternate instruction form stored in the buffers." Further, at page 11, line 21, "The sequencer is invoked by an unconditional branch instruction (e.g., branch_to_C$) detected by the decode/issue/branch

mechanism, 323/324/305, of the primary instruction form. The branch instruction suspends primary instruction fetch/decode/issue/execute functions and enables the alternate mechanism of the sequencer 325." The instructions of a second form, statically loaded in the buffers, execute in fewer cycles due to the reduction in branch penalty without the need for branch prediction and target prefetch mechanisms (see page 11, lines 8-11). Accordingly, the branch instruction is believed to be adequately described. The Examiner's reconsideration of the objection is respectfully requested.

The Examiner indicated that a grammatical error appears at page 12, line 8. The paragraph has been amended to correct the error. Reconsideration of the objection is respectfully requested.

Claims 12 and 21 have been objection to as including inherent limitations not claimed. Claims 12 and 21 have been amended to clarify the limitations of the claimed processor. Reconsideration of the objection is respectfully requested.

Claims 15 and 18 have been objection to as including the phrase "a buffer" and depending on a claim reciting "a plurality of buffers." Claims 15 and 18 have been amended to clarify "a buffer" as being of the "plurality of buffers." The Examiner's reconsideration of the objection is respectfully requested.

Claims 1 and 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni (U.S. Patent No. 6,223,254) in view of Chan (U.S. Patent No. 5,317,745). The Examiner stated essentially that the combined teachings of Soni and Chan teach or suggest all the limitations of claims 1 and 5-9.

Claim 1 claims, *inter alia*, "storing a plurality of instructions of the second form in a plurality of buffers proximate to a plurality of execution units; executing at least one instruction of the first instruction form in response to a first counter; and executing at least one instruction of

the second instruction form in response to at least a second counter, wherein the second counter is invoked by a branch instruction of the first instruction form."

Soni teaches a parcel cache for storing decoded instructions (see Abstract). Soni does not teach or suggest "executing at least one instruction of the second instruction form in response to at least a second counter, wherein the second counter is invoked by a branch instruction of the first instruction form" a claimed in claim 1. As suggested by the Examiner, Soni does not teach a second counter, wherein the second counter is invoked by a branch instruction of the first form. Soni teaches that one general purpose register is used as a counter (see col. 8, lines 17-19). Further, nowhere does Soni teach or suggest that the counter is invoked by a branch instruction. Soni does not teach or suggest a second counter. Therefore, Soni fails to teach or suggest all the limitations of claim 1.

Chan teaches a program counter apparatus for reducing latency times, wherein multiple program counters are used in conjunction with multiple interrupt devices (see Abstract and col. 3, lines 6-18). Chan does not teach or suggest "executing at least one instruction of the second instruction form in response to at least a second counter, wherein the second counter is invoked by a branch instruction of the first instruction form" a claimed in claim 1. Chan teaches that program counters correspond to interrupt devices, and that the program counters are invoked by a control logic receiving interrupt signals (see col. 4, lines 20, 29). More particularly, the program counters function in response to a flag set (see col. 4, lines 33-35). Nowhere does Chan teach or suggest that the alternate program counters are invoked by a branch instruction. The flag set of Chan is not an instruction, much less a branch instruction. Therefore, Chan fails to sure the deficiencies of Soni.

The combined teachings of Soni and Chan fail to teach or suggest "executing at least one

instruction of the second instruction form in response to at least a second counter, wherein the second counter is invoked by a branch instruction of the first instruction form" a claimed in claim 1.

Further, with respect to claim 1, the Examiner has taken Official Notice that it is well known and expected in the art that a buffer split into a plurality of smaller buffers has the benefit of less complex indexing circuitry leading to faster lookups. Applicants respectfully traverse the finding of Official Notice. Merely splitting a single buffer into a number of smaller buffers is not believed to reduce the total size of the buffer needed to be searched for contents. Thus, the time needed to perform a lookup in a single buffer or a plurality of buffers having a total size similar to the single buffer would be substantially the same if not more considering the time needed for switching between the plurality of buffers. Therefore, using multiple buffers would not be an obvious alternative to a single buffer. If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. Such an affidavit is respectfully requested.

Claims 5-9 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. At least claims 8 and 9 are believed to be allowable for additional reasons.

Claims 8 and 9 recites, *inter alia*, "a buffer of a branch unit."

Soni teaches a parcel cache for storing decoded instructions (see Abstract). Soni does not teach or suggest "a buffer of a branch unit" a claimed in claims 8 and 9. Soni teaches that a parcel cache is coupled to the fetch/parse/decide/issue unit 43, and sends parcels to a reservation station (see col. 7, lines 19-20 and col. 9, lines 31-34). Nowhere does Soni teach or suggest that a

branch unit has a buffer. Therefore, Soni fails to teach or suggest all the limitations of claims 8 and 9.

Chan teaches a program counter apparatus for reducing latency times, wherein multiple program counters are used in conjunction with multiple interrupt devices (see Abstract and col. 3, lines 6-18). Chan does not teach or suggest "a buffer of a branch unit" a claimed in claims 8 and 9. Chan teaches that a buffer is used for storing an address of an interrupted program (see col. 1, lines 19-22). However, nowhere does Chan teach or suggest that the buffer is of a branch unit. Therefore, Chan fails to sure the deficiencies of Soni.

The combined teachings of Soni and Chan fail to teach or suggest a buffer of a branch unit, as claimed in claims 8 and 9. For the foregoing reasons, the Examiner's reconsideration of the rejection is respectfully requested.

Claims 2 and 3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Chan, as applied to claims 1 and 5-9, and further in view of Ball and Larus ("Efficient Path Profiling," 29th Annual IEEE/ACM International Symposium on Microarchitecture, Paris, pp. 46-57, 1996.) The Examiner stated essentially that the combined teachings of Soni, Chan and Ball teach or suggest all the limitations of claims 2 and 3.

Claims 2 and 3 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. At least claim 2 is believed to be allowable for additional reasons.

Claim 2 claims, *inter alia*, "wherein instructions of the second form are statically loaded into the plurality of buffers."

Soni teaches a parcel cache in which parcels are replaced by a least recently used algorithm (see col. 12, lines 25-27). Soni does not teach or suggest instructions of the second form

statically loaded into the plurality of buffers, essentially as claimed in claim 2. Soni teaches that the contents of the parcel buffer are replaced as a program executes. Thus, the parcel buffer of Soni is not statically stored with instruction. Therefore, Soni fails to teach or suggest all the limitations of claim 2.

Chan teaches a program counter apparatus for reducing latency times, wherein multiple program counters are used in conjunction with multiple interrupt devices (see Abstract and col. 3, lines 6-18). Chan does not teach or suggest that "instructions of the second form are statically loaded into the plurality of buffers" as claimed in claim 2. Chan teaches that a buffer is used for storing an address or an interrupted program (see col. 1, lines 19-22). The contents of the buffer therefore change as the program is repeatedly interrupted by different devices. Further, an address of an interrupted program is not an instruction. Therefore, Chan does not teach or suggest that "instructions of the second form are statically loaded into the plurality of buffers" as claimed in claim 2. Therefore, Chan fails to cure the deficiencies of Soni.

Ball teaches program profiling (see Abstract). Ball does not teach or suggest that "instructions of the second form are statically loaded into the plurality of buffers" as claimed in claim 2. Ball teaches a path profiling algorithm for identifying sets of potential paths with states, which are encoded as integers (see page 47, Algorithm Overview). Ball does not teach or suggest a processor architecture, much less instructions statically loaded into the plurality of buffers, essentially as claimed in claim 2. Therefore Ball fails to cure the deficiencies of Soni and Chan.

The combined teachings of Soni, Chan and Ball fail to teach or suggest that "instructions of the second form are statically loaded into the plurality of buffers" as claimed in claim 2. Reconsideration of the rejection is respectfully requested.

Claims 4 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over

Soni in view of Chan, as applied to claims 1 and 5-9, and further in view of Johnson ("Superscalar Microprocessor Design," Prentice Hall 1991). The Examiner stated essentially that the combined teachings of Soni, Chan and Johnson teach or suggest all the limitations of claims 4 and 10.

Claims 4 and 10 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 11, 13 and 16-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni. The Examiner stated essentially that the teachings of Soni teach or suggest all the limitations of claims 11, 13 and 16-20.

Claim 11 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing the decoded instructions of the first instruction form and the plurality of execution units."

Soni teaches a parcel cache for storing decoded instructions coupled to an instruction streaming buffer, a decoded instruction queue and a reservation station (see Abstract and Figure 3). Soni does not teach or suggest that a "sequencer controls a plurality of gates connected between a plurality of execution queues for storing the decoded instructions of the first instruction form and the plurality of execution units" as claimed in claim 11. Soni teaches that the execution units are coupled to the reservation station (see Figure 3). Soni does not teach or suggest a gate between the reservation station and the execution units. Therefore, Soni does not teach or suggest a sequencer for controlling a plurality of gates connected between a plurality of execution queues and the plurality of execution units, essentially as claimed in claim 11.

Therefore, Soni fails to teach or suggest all the limitations of claim 11.

Claims 13 and 16-20 depend from claim 11. The dependent claims are believed to be allowable for at least the reasons given for claim 11. At least claim 20 is believed to be allowable for additional reasons.

Claim 20 claims, "wherein the second instruction form is a logical subset of the first instruction form, wherein the predecoded instructions of the second instruction form are statically stored in the plurality of buffers."

Soni teaches a parcel cache in which parcels are replaced by a least recently used algorithm (see col. 12, lines 25-27). Soni does not teach or suggest predecoded instructions of a second instruction form statically stored in a plurality of buffers, essentially as claimed in claim 20. Soni teaches that the contents of the parcel buffer are replaced as a program executes (see col. 12, lines 25-27). Thus, Soni does not teach or suggest a static buffer. Therefore, Soni fails to teach or suggest all the limitations of claim 20. The Examiner's reconsideration of the rejection is respectfully requested.

Claim 12 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni as applied to claims 11, 13 and 16-20, and further in view of Ball. The Examiner stated essentially that the combined teachings of Soni and Ball teach or suggest all the limitations of claim 12.

Claim 12 depends from claim 11. Claim 12 is believed to be allowable for at least the reasons given for claim 11. Reconsideration of the rejection is respectfully requested.

Claims 14 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni as applied to claims 11, 13 and 16-20, and further in view of Johnson. The Examiner stated essentially that the combined teachings of Soni and Johnson teach or suggest all the limitations of claims 14 and 15.

Claims 14 and 15 depend from claim 11. The dependent claims are believed to be allowable for at least the reasons given for claim 11. Reconsideration of the rejection is respectfully requested.

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni, in view of Ball and Johnson. The Examiner stated essentially that the combined teachings of Soni, Ball and Johnson teach or suggest all the limitations of claim 21.

Claim 21 claims, *inter alia*, "a plurality of buffers, proximate to the execution units, for statically storing predecoded instructions of the second instruction form, wherein each execution unit is connected to a corresponding buffer of the plurality of buffers."

Soni teaches a parcel cache in which parcels are replaced by a least recently used algorithm (see col. 12, lines 25-27). Soni does not teach or suggest "a plurality of buffers, proximate to the execution units, for statically storing predecoded instructions of the second instruction form", as claimed in claim 21. Soni teaches that the contents of the parcel buffer are replaced as a program executes (see col. 12, lines 25-27). Soni does not teach or suggest statically storing predecoded instructions, essentially as claimed in claim 21. Therefore, Soni fails to teach or suggest all the limitations of claim 21.

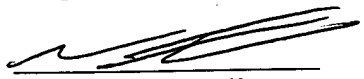
Ball teaches program profiling (see Abstract). Ball does not teach or suggest "a plurality of buffers, proximate to the execution units, for statically storing predecoded instructions of the second instruction form" as claimed in claim 21. Ball teaches a path profiling algorithm for identifying sets of potential paths with states, which are encoded as integers (see page 47, Algorithm Overview). Ball does not teach or suggest a processor architecture, much less a buffer for statically storing predecoded instructions, essentially as claimed in claim 21. Therefore Ball fails to cure the deficiencies of Soni.

Johnson teaches a central window as an alternative to reservation stations (see page 134). Johnson does not teach or suggest "a plurality of buffers, proximate to the execution units, for statically storing predecoded instructions of the second instruction form", as claimed in claim 21. The reservation stations of Johnson include allocation and deallocation routines (see page 134, lines 12-13). Thus, the reservation stations of Johnson are not static. Johnson does not teach or suggest a buffer statically storing predecoded instructions, essentially as claimed in claim 21. Therefore, Johnson fails to cure the deficiencies of Soni and Ball.

The combined teachings of Soni, Ball and Johnson fail to teach or suggest "a plurality of buffers, proximate to the execution units, for statically storing predecoded instructions of the second instruction form" as claimed in claim 21. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-21, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,



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Annotated Sheet

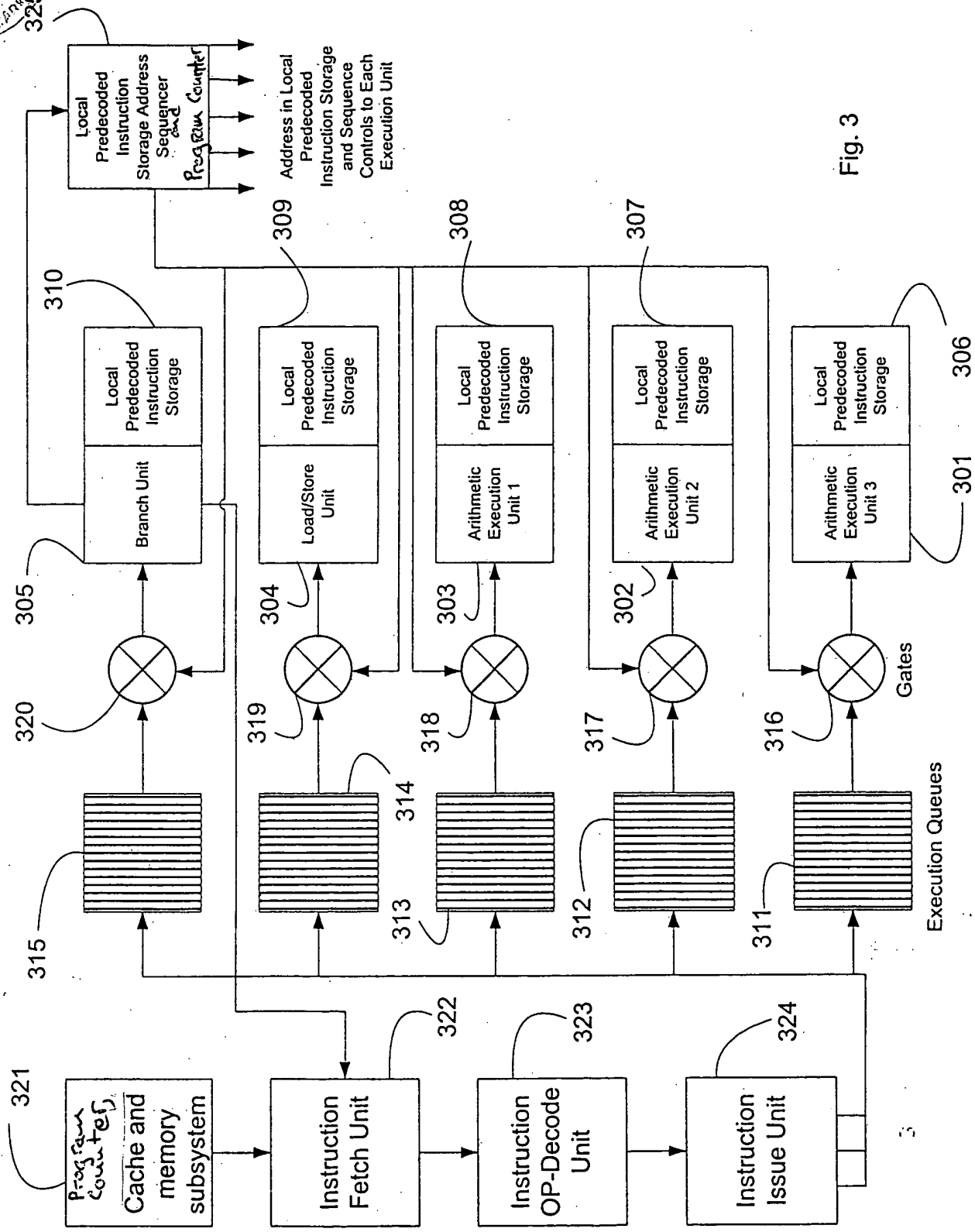

Fig. 3